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# A T-Type Direct AC/AC Converter Structure

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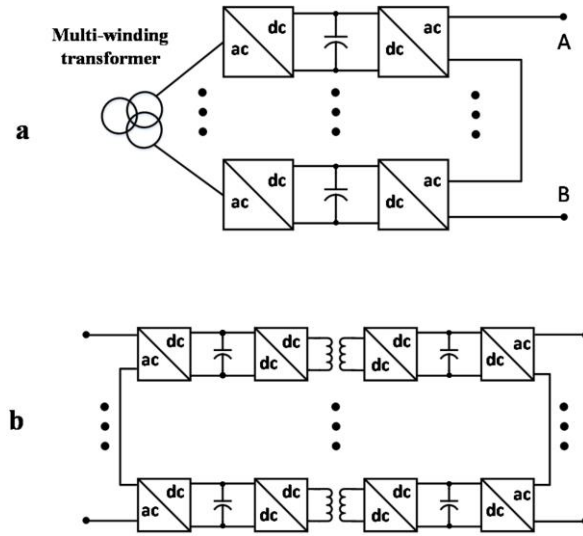
**Abstract:** In this paper a novel T-type topology for 1-phase direct AC/AC conversion is proposed. In this topology, frequency changing takes place directly (without common DC voltage bus) through three converters that are connected in a T structure. Unity input power factor and precise output voltage and frequency regulation is achieved through appropriate control of these three converters. H-bridge converters can be used in each branch of T to make the proposed converter. The converter is controlled such that the average active power of each H-bridge remains zero. Therefore, capacitors are implemented in DC links of H-bridges. Moreover, using half-bridge converters, instead of H-bridge ones, for T branch converters, leads to an AC/AC converter with only six semiconductor switches. Also, multilevel inverters, specially cascaded H-bridge can be used in branches of T. This will lead to a multilevel AC/AC converter that is suitable for high power applications such as intertie connections and high power motor drives. Principle of operation and control schemes of the converter are then explained. Simulation and experimental results verify the performance of the converter while operating as a power supply at different frequencies.

## 1. Introduction

Electric motor drives and loads which need to be supplied by special frequencies e.g. 25Hz, 150Hz or 400Hz are utilizing AC/AC converters [1], [2]. AC/AC converters should be able to not only change the frequency but also set the amplitude of voltage to a desired level with adequate regulation. AC/AC converters can be generally classified into direct [3-8] and indirect [9-12] structures.

Cycloconverter is one of the earliest known topologies for direct AC/AC conversion which is simple but suffers from low frequency harmonics [3]. Matrix converters [4] are another form of direct AC/AC converters that have received considerable attention due to their potentiality to provide direct AC/AC conversion without energy storage component [5]-[7]. However, they never turned into wide application due to some drawbacks and restrictions like their need to four-quadrant switches, having critical timing, requiring measurement of switch voltage and current, complicated snubber circuits and their voltage boosting restriction [9].

Indirect AC/DC/AC conversion by means of PWM rectifier-inverter systems with DC voltage/current link are widely used for AC to AC conversion. As compared to matrix converters,



**Fig. 1** conventional CHB Back-to-Back Converters.  
 a Using multi-winding transformer,  
 b Using insulated dc/dc converter

these systems show improved reliability and allow a greater output voltage. They use unidirectional switches; moreover, a capacitor/inductor in the DC link provides decoupling between the rectifier and the inverter, so that the two converters can be driven independently using PWM techniques like SPWM or SVM [10-12], providing excellent input and output performances.

Due to current technological restrictions on semiconductor switches, high power AC-AC application is achieved through multilevel converters in both direct and indirect AC-AC topologies e.g. Modular Multilevel Matrix Converter ( $M^3C$ ) [13]. A chainlink based matrix converter which is capable of producing AC output by using unipolar submodules is presented in [14]. Hexverter, using six branches of Modular Multilevel Converter (MMC) for three-phase AC-AC system, is surveyed in [15]. In [16] a Hexverter arisen by omitting DC-link of back-to-back modular multilevel converter is presented. Existence of weak side-to-side decouple in addition to large DC capacitors and arm inductors, however, imposes some constrains on Hexverter topology. In [17] a three-phase hexagonal chopper system known as modular multilevel AC hexagonal chopper ( $M^2AHC$ ) is developed. Although the proposed hexagonal chopper carries out AC-AC conversion small footprint and less control complexity, lack of side-to-side decouple is one of its drawbacks.

As mentioned in the previous paragraphs, indirect AC/DC/AC converter which is created by cascading a four-switch rectifier with a four-switch inverter and an electrolytic capacitor in the DC link in its single phase structure, is the most popular converter for frequency changing goals. As power increases, voltage/current stress of switches will increase. In order to reach higher voltages and powers, multilevel converters like Cascaded H-Bridge (CHB) can be used. However, back-to-back CHB needs an isolated dc link for each converter cell in order to prevent DC link short circuit

[18-19]. For isolation, normally, multi-winding primary transformer are used, as depicted in Fig. 1a which has been used by Gamesa in their 4.5-MW project [20] and Siemens in some of multi-MW projects [22]. Bulky and massive low-frequency transformer increases the weight and volume of the converter [22], [23]. As shown in Fig. 1b, galvanic insulated DC/DC converters as interface is another solution which shares a similar idea with some of the next generation traction converters [24], [25], as well as the European UNIFLEX-PM project [26].

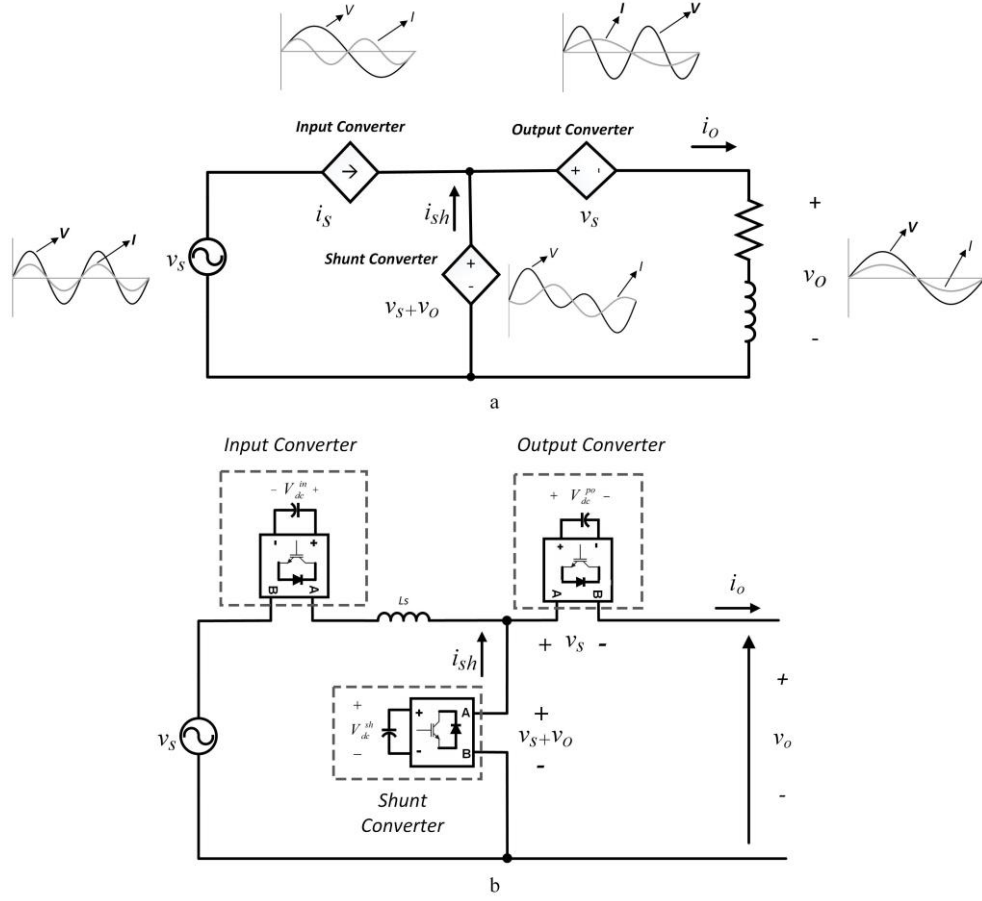
In this paper, a novel topology is introduced in which not only are the capacitor current ripples halved, but also, in the multilevel structure, the bulky, massive, and costly line-frequency transformer is omitted. The principle of operation of the proposed topology is analysed in section 2 via a simplified ideal model of the converter. A control method is described in section 3 in order to realize the ideal model. Finally, in sections 4 and 5, simulation and experimental results verify the structure and its control scheme.

## 2. Principle of operation

The basic operation of the proposed topology is described in this section. In the first step, to simplify the understanding of the converter operation, converter and its control are assumed to be ideal. Fig. 2a shows the structure of ideal representation of the proposed converter, which is consisted of a controlled current source and two controlled voltage source. In the next step, these ideal sources are replaced by properly controlled switching converters. Hereafter, these sources will be called as Input Converter, Shunt Converter, and Output Converter as depicted in Fig. 2a. The active power in a multi frequency system is defined as the product of in-phase voltages and currents of the same frequency, as in (1):

$$P = \sum_{n=1}^{\infty} V_n I_n \cos(\varphi_n) \quad (1)$$

Where  $I_n$  and  $V_n$  are the RMS values of the  $n$ -th harmonic current and voltage, respectively, and  $\varphi_n$  is the voltage and current phase difference. To have unity power factor in the input port of the frequency changing converter, source current should be regulated. To have a variable voltage and frequency output on the load side, output voltage and frequency should be regulated. These can be



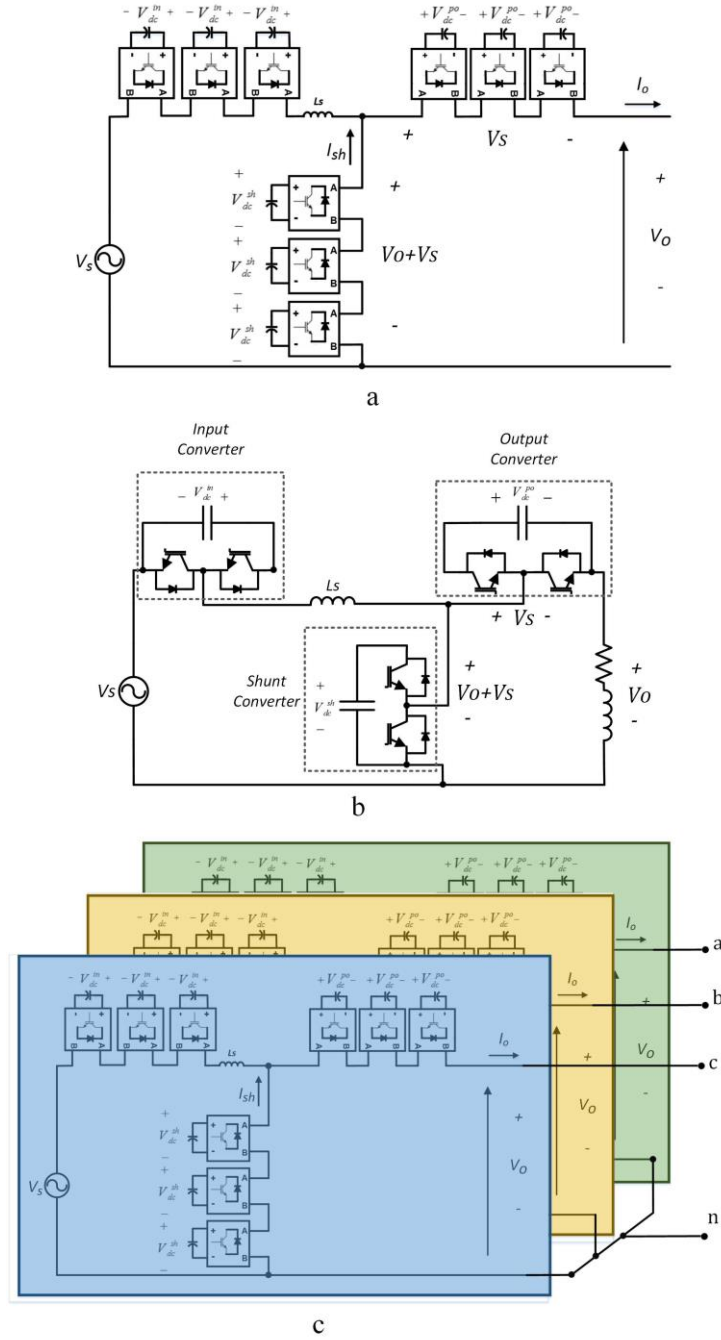
**Fig. 2.** Proposed topology:

*a* Ideal model of the proposed ac/ac converter. Current and voltage waveforms of each branches are illustrated beside it.  
*b* Realization of the converter by using H-bridges

achieved through control of ideal sources of Fig. 2a. The energy delivered by the input source in the input terminal of T converter with a voltage of  $v_s$  and a frequency of  $f_s$ , should be delivered to the load at the output terminal of T converter with a voltage of  $v_o$  and a frequency of  $f_o$ . Frequency changing takes place in dependent sources of branches of T while the average power delivered/absorbed by each controlled voltage/current source is zero. Therefore, no energy is exchanged between dependent sources and the rest of converter. To achieve this goal, values of dependent sources, shown in Fig. 2a, are set as follows:

To respect KVL and KCL beside aforementioned requirements, the Output Converter should be a dependent voltage source at the value of  $v_s$ . The Shunt Converter operates as a dependent voltage source which its value is fixed at  $v_s + v_o$ . The Input Converter acts as a dependent current source at the value of  $i_s$ , which is a current at frequency of  $f_s$ .

By using KVL in the circuit shown in Fig. 2a, the voltage and current of Input Converter and



**Fig. 3.** Proposed T-type ac/ac converter:  
a Multilevel version of proposed converter  
b Half-bridge version  
c Three-phase Y-connection structure

Output Converter are fixed at different frequencies and according to (1), their average active power is zero. Using (1), the active power of the Shunt Converter is calculated as:

$$P_{sh} = V_s I_s \cos \varphi_s - V_o I_o \cos \varphi_o \quad (2)$$

The net active power of Shunt Converter must be zero to exchange no energy with the rest of the system. The Shunt Converter is, therefore, required to draw a current component from the supply so that it balances the power demanded by the load. So, for steady state operation the  $I_s \cos \varphi_s$  should set  $P_{sh}$  to zero. Hence:

$$I_s \cos \varphi_s = \frac{V_o I_o \cos \varphi_o}{V_s} \quad (3)$$

In order to reach unity power factor  $\cos \varphi_s$  sets to one, so  $I_s$  is calculated as (4):

$$I_s = \frac{V_o I_o \cos \varphi_o}{V_s} \quad (4)$$

Therefore all Input, Output, and Shunt Converter must be controlled to exchange zero active power with the load; otherwise the cell capacitor will discharge or over charge.

To illustrate the operation of the proposed converter, Fig. 2a, also shows the voltage and current waveforms in all converter branches for a given operation condition. The voltage and current waveforms of each branch are shown beside it. The load frequency is set to half of the supply frequency (considering the converter is supplied from a 50-Hz supply and desired output frequency is 25-Hz). It can be verified that due to voltage and current frequency mismatch, the average active power of each converter is zero.

Fig. 2b shows the realization of the ideal circuit by means of using H-bridge converter, substituted by its corresponding ideal source. Based on the power rating, half-bridge, H-bridge and multilevel converters can be used to realize each controlled sources of Fig. 2a. The simplest realization is to use one H-bridge in each branch of T that is suitable for low/medium power applications as shown in Fig. 2b. It is worth mentioning that since the average active power of each branch is zero, capacitors rather than independent DC sources can be used in DC link of the converter.

The inductor in Input Converter ( $L_s$ ) is an interface reactor which, likewise that of STATCOM, is added to reduce current ripples due to the switching [27-29]. In comparison with the other voltages, the inductor voltage is small, and, therefore, its effect is neglected in analysis of the converter.

Thus, as in a STATCOM, neglecting converter losses, each H-bridge module, and hence each branch, is constrained to exchange no energy with rest of the system in order to avoid discharge or

overcharge of capacitor voltages.

From another point of view, for high power applications, instead of using an H-bridge in each branch, series string of H-bridges can be assigned to make a cascaded multilevel converter in each branches of T. For example, as shown in Fig. 3a, 7-level version of the proposed T converter is configured through implementation of three H-bridge modules in each branches of T. Control scheme for this version of converter is akin to cascaded multilevel star connected STATCOMs [30] and is explained in the next section. Capacitors are placed in DC link of each H-bridges and capacitor voltages are regulated at desired references.

The third version of the proposed T converter is arisen for the purpose of reducing the cost and the number of semiconductor switches of the converter using half-bridge inverters. One of the drawbacks of using half-bridges in power electronics converters is the existence of DC voltage component in addition to desired AC voltage in the AC side of the inverter. But in the proposed topology, considering equal DC link voltages in this case, the mentioned DC component is omitted in the loops by KVL. As shown in Fig. 3b, using half-bridge inverters, a 1-phase AC/AC converter with only six switches is realized. The DC component of the Shunt Converter is omitted by the DC component of the Output Converter, so  $v_o$  is a pure AC voltage at the desired frequency. Also, using KVL in the input side of the converter of Fig. 3b, it can be verified that the DC component of the Shunt Converter is omitted by the DC component of Input Converter.

The proposed topology is capable to be exploited for high-power application, so much so that, the three-phase Y-connection structure of the converter is demonstrated in Fig. 3c.

As will be explained in section 3, the control strategies are developed to modify the input power factor, despite capacitive/inductive load.

### **3. Modulation and control of the converter**

This section develops suitable control strategies to regulate the capacitor voltages in all three converters, control the current of the Input Converter, and set the output voltages of the Shunt and Output Converters. This section also develops control strategies for both 2-level and multi-level version of the proposed topology.

#### *3.1 Control of Two-level Version of Converter*

Using bipolar switching technique for each H-bridge of Fig. 2b produces two-level waveform while using unipolar one will brings about three-level waveforms. In the simulation, the former is used. In controlling the converter topology of Fig. 2b, one of the main issues is regulation of



capacitor voltages. Balance of energy between the supply and load power is an implicit requirement for the controller.

As long as conventional inverters are concerned, the output voltage is achieved by the following rule—in which  $m_a$  is modulation index and  $V_{dc}$  is voltage of DC-link:

$$v_{ac} = V_{dc} m_a \sin(\omega t) \quad (5)$$

The Output Converter and Shunt Converter are controlled as voltage-controlled voltage source inverters (VSI); therefore, by using simple PWM modulator, as shown in Fig. 4a and Fig. 4b, these two converters can be controlled. Since sawtooth signals (modulator signals) assumed to be between 0 and 1, gains of  $1/V_{dc}^{po}$  and  $1/V_{dc}^{sh}$  is mandatory to project the reference signals between 0-1 to avoid over-modulation ( $m_a > 1$ ).

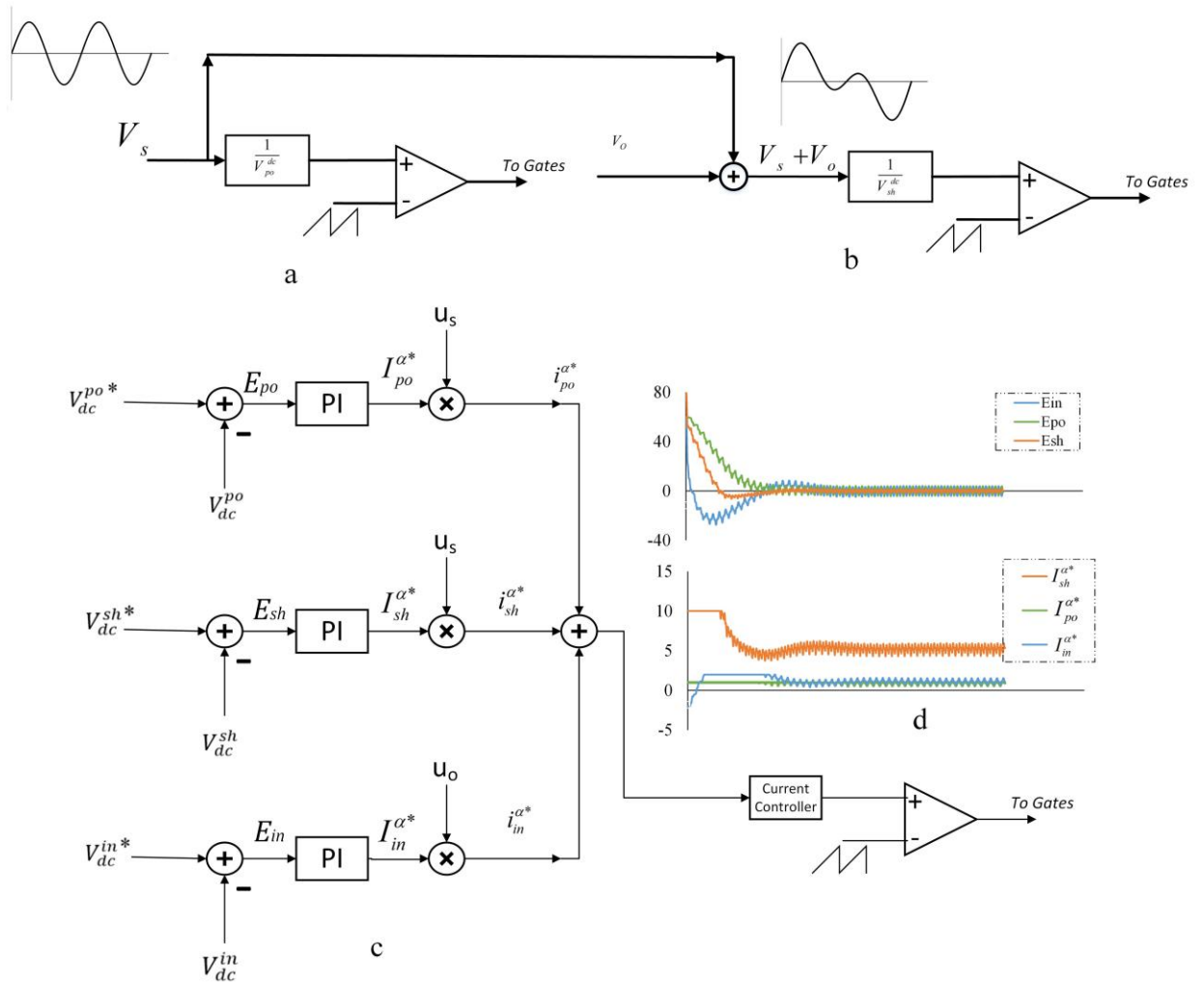
The control scheme for the Input Converter is a little more complex. The control of the Input Converter is similar to current controlling of a VSI and also is akin to regulation of capacitor DC voltage of a STATCOM. As illustrated in Fig. 4c, there are three capacitor voltage regulators (PI controller) that adjust the DC link voltages to their desired value and eliminate the error between reference value and measured value of voltage capacitor. The output of each PI controller is multiplied by a unity sine wave that is at proper frequency and proper phase accordingly. Due to the requirement of active power (energy) to regulate the capacitor voltages, this frequency and phase difference is chosen to transfer active power to compensate the switching and other losses. For instance, voltage across the Output Converter is at  $f_s$  so the PI block output is multiplied to  $u_s$  (unity amplitude sine wave at frequency of  $f_s$ ).

In Fig. 4,  $u_s$  and  $u_o$  are sinusoidal signals of unity amplitude which are, respectively, in phase to  $v_s$  and in phase to  $v_o$ . Like control strategy that is developed for balancing of voltage capacitor of STATCOM, PR controller is a suitable controller for current regulation goals because it can eliminate sinusoidal errors where the references are sinusoidal. Tracking of the reference current,  $i_{in}^*$ , is accomplished by a PR current controller [31]. In order to clarify the operation of controller, in general, and the role of each components in Fig. 4c, in particular, simulation of some vital interior signals is shown in Fig. 4d. Regulation of capacitor voltage at a desire value is the main task of the controller; therefore, error signals— $E_{in}$ ,  $E_{po}$ , and  $E_{sh}$ —are shown to reach zero in steady state. The actuators that cause this task (elimination of errors) are output signals of PI controllers that are, in fact, current amplitudes of each branch that will be multiplied by appropriate sine waveform— $u_s$  and  $u_o$ —to deliver or draw active power (energy) to/from capacitors to regulate their voltages. These

signals are depicted in Fig. 4d as  $I_{in}^{\alpha*}$ ,  $I_{sh}^{\alpha*}$ , and  $I_{po}^{\alpha*}$ .

As depicted in Fig. 4d,  $I_{in}^{\alpha*}$  and  $I_{po}^{\alpha*}$  are stabilized at small current values which is used to compensate losses due to switching and etc. If ideal form of each components is substituted, this values reach zero at steady state. On the other hand, the output signal of Shunt Converter PI controller,  $I_{sh}^{\alpha*}$ , is stabilized at significant higher value. The values is, in fact, the amount of current that flows through Shunt Converter at the source frequency,  $f_s$  ; and subsequently; from Input Converter and is drawn from the source:  $I_s$ . Therefore, this current, as explained in section 2, balances active power between source and load. The more energy consumed at load, the more  $I_s$  is needed, and the more energy is draw from the source.

The aforementioned control strategy and corresponding scheme of Fig. 4 is utilized for off-



**Fig. 4** Control Block for the proposed Converter.

*a* Control scheme of Output Converter,

*b* Control scheme of Shunt Converter,

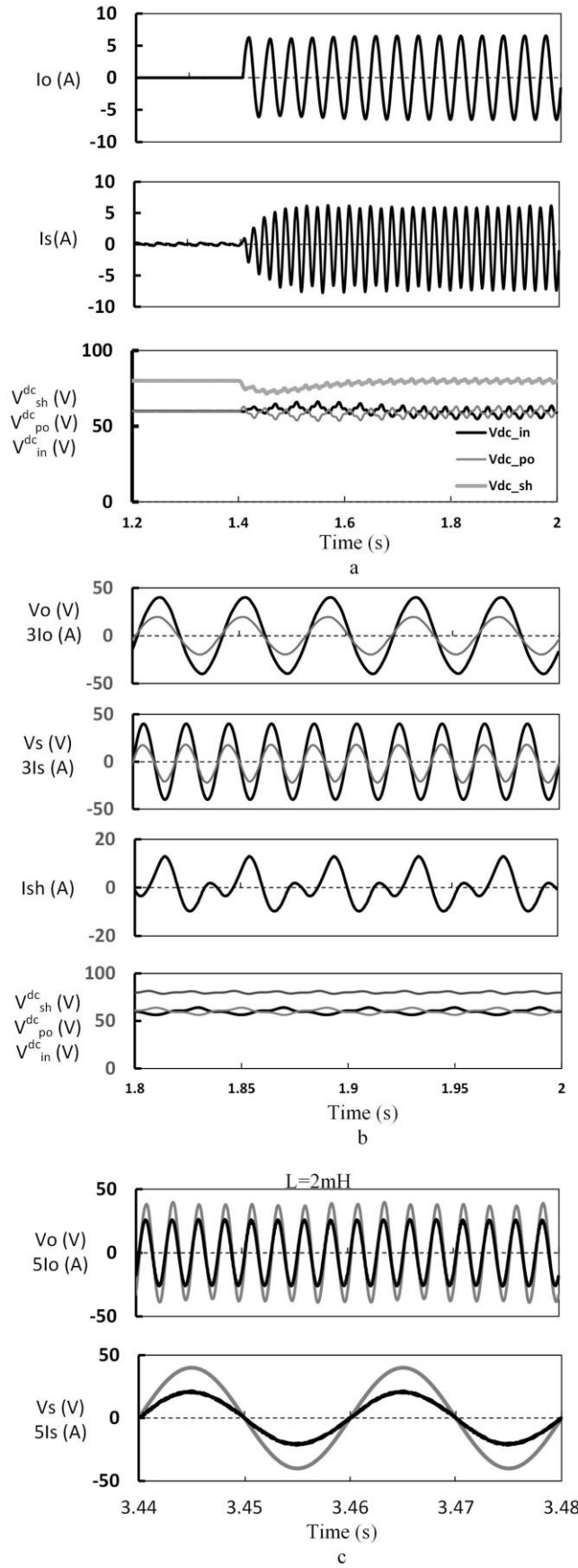
*c* Control scheme of Input Converter,

*d* Simulation of some control signals

grid loads. In order to exploit the proposed converter as a grid-connected one, some changes are supposed to be accomplished in control strategy. The Output Converter control should be altered to current control instead of voltage control. In fact, desirable current that is injected to the grid is introduced as reference value to the control block diagram of Output Converter. Due to avoid distraction from major concept, more elaborated explanation about grid-connected scheme is not mentioned in this paper.

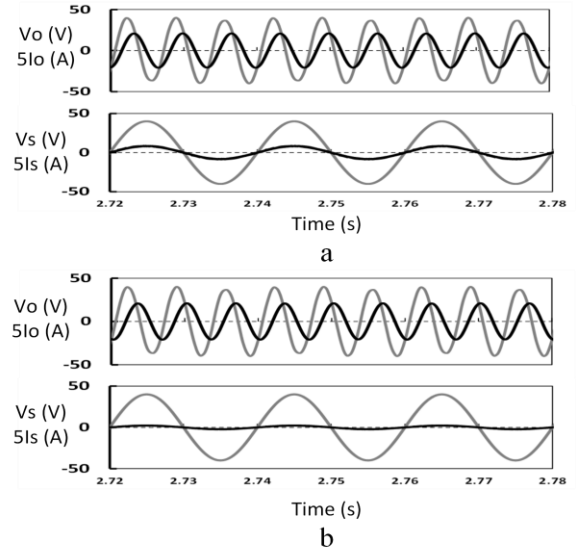
### 3.2 Control of Multi-level Version of Converter

The control scheme for Output Converter and Shunt Converter for the case of multilevel structure is similar to the 2-level type of the converter, as mentioned in the previous section. There are two solutions to



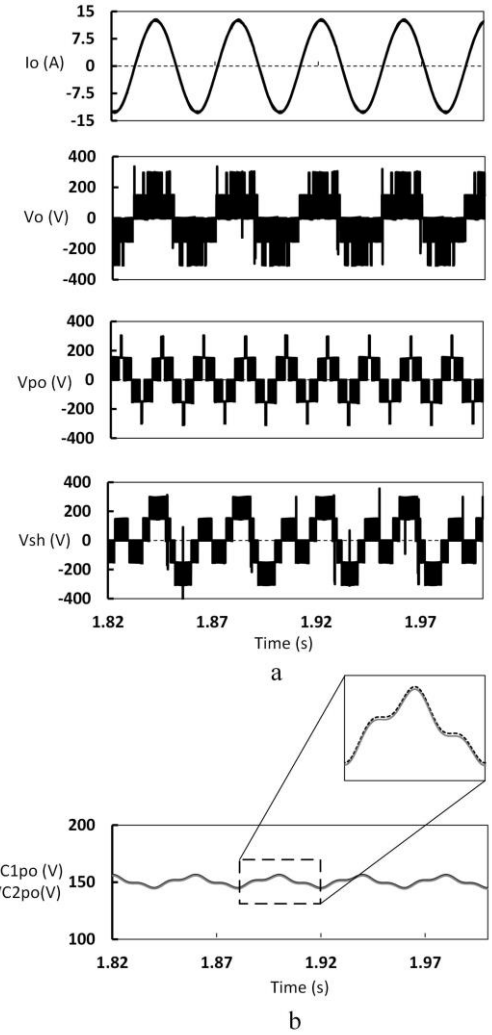
**Fig. 5.** Results for

- a Load impact at output frequency of 25 Hz
- b Steady state at output frequency of 25 Hz
- c Steady state at output frequency of 400 Hz



**Fig. 6.** Output/Input Current/Voltage for 150Hz

- a R-L load
- b Inductive load



**Fig. 7.** Simulation Results for Multilevel version of the proposed converter

- a Waveforms in terms of output current ( $I_o$ ), output voltage ( $V_o$ ), voltage across Output Converter ( $V_{po}$ ), voltage across Shunt Converter ( $V_{sh}$ )
- b Capacitor voltage balancing of Output Converter

achieve modulation: generic PWM technique and staircase modulation. Although staircase modulation has merits such as lower switching frequency and lower semiconductor losses, but in this case generic PWM techniques are used because what is needed for correct operation of the converter is, indeed, lower harmonics of converter voltage rather than high frequency harmonics. These high frequency harmonics is filtered readily. In addition, even though using of staircase modulation appears staircase waveform across both of Output and Shunt Converter, and also it is possible to utilize techniques such as Selected Harmonics Elimination) SHE to diminish THD, but there is no guarantee to assure that the output voltage, which is aggregation of both of them, has a suitable staircase waveform that despite of correct operation of the converter, it has the minimum THD. In other words, despite of using a modulation technique e.g. SHE to reduced voltage THD of Shunt and Output Converter, the output voltage may not enjoy SHE. So the generic PWM is used. Phase-shift [32] or level shift [33] multilevel modulation strategies can be used to create switches gate signals.

In multilevel type of the converter, in addition to overall capacitor voltage regulation of each branch, the voltage balancing between cascade converters of each branch is an important issue. Using control block of Fig. 4c regulate the overall capacitor voltages of each branch while balancing of each individual cell capacitor is supposed to be achieved; therefore, control blocks should be extended to achieve capacitor voltage balancing. The control scheme is similar to the one in Fig. 4 plus adding some quadratic component current to  $i_{in}^*$ , in order to balance voltages of each cascade H-bridge [30, 34-36]. The operation of the rest of the control blocks is similar to 2-level type. Each cell capacitor uses its own PI controller and the output signal of PI block is multiplied by a sine wave which is 90 degrees leads from  $u_s$  or  $u_o$ . This control strategy is proved in [30] and also works well for this topology. Furthermore, in order to enhance the control performance, some control techniques can be used [37].

#### 4. Simulation results

To validate the proposed topology, and associated control strategies, a single-phase simulation is carried out for 2-level H-bridge and 5-level topology and a 2-level half-bridge topology. Simulations are conducted for output frequency of 25 Hz. To prove the ability of the proposed converter in frequency augmentation, the output frequency of 400 Hz and 150Hz are tested. The parameters and the ratings of simulation and experimental prototype are listed in Table 1.

The selection of capacitor values mainly depends on several parameters such as: the current

that flows through it, low frequency of this current rather than high frequency harmonics, the DC voltage across it, and the acceptable voltage ripple. Therefore, to reach a specific value for the capacitors some formulas should be considered as follows: the instantaneous power of DC side and AC side of a H-bridge is assumed to be equal, consider Output Converter, for instance, so

$$\frac{dW}{dt} = v_{po} i_o \quad (6)$$

Where  $W$  is the energy that stores in a capacitor and is defined as

$$W = \frac{C_{po}}{2} (V_{dc}^{po})^2 \quad (7)$$

So, by substituting (7) in (6):

$$C_{po} V_{dc}^{po} \frac{dv_{dc}^{po}}{dt} = V_{po} I_{po} (\cos(\omega_o t - \omega_s t + \varphi) + \cos(\omega_o t + \omega_s t + \varphi)) \quad (8)$$

Thus,

$$v_{dc}^{po}(t) = \frac{V_{po} I_{po}}{C_{po} V_{dc}^{po}} \left( \frac{1}{\omega_o - \omega_s} \sin(\omega_o t - \omega_s t + \varphi) + \frac{1}{\omega_o + \omega_s} \sin(\omega_o t + \omega_s t + \varphi) \right) \quad (9)$$

Both the maximum and minimum possible value of the above sine term is computable since the maximum and minimum of  $\sin(\omega t)$  are 1 and -1, respectively. So the ripple of capacitor voltage is:

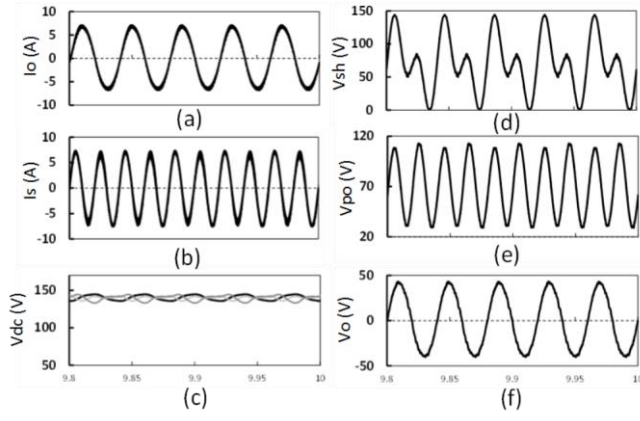
$$\Delta V_{dc}^{po} = \frac{2V_{po} I_{po}}{C_{po} V_{dc}^{po}} \left( \frac{1}{\omega_o - \omega_s} + \frac{1}{\omega_o + \omega_s} \right) \quad (10)$$

Where  $\Delta V_{dc}^{po}$  is voltage ripple across capacitor. Using (11), the effect of each parameter that contributes to the value of capacitor is measurable.

$$C_{po} = \frac{2V_{po} I_{po}}{\Delta V_{dc}^{po} V_{dc}^{po}} \left( \frac{1}{\omega_o - \omega_s} + \frac{1}{\omega_o + \omega_s} \right) \quad (11)$$

#### 4.1 Simulation Results for 2-level H-Bridge Type During Load Variation and Steady State Operation

To show the dynamic performance of the converter, a switched R-L load is used to apply load steps from zero to full load. The system response for the case of 25-Hz output voltage is shown in Fig. 5a. This figure shows the voltage and current waveforms of load and source, and all capacitor voltages under load variation. As shown in Fig. 5a, at the moment of starting switch, the output current ( $I_o$ ) is reached its nominal value while the source current ( $I_s$ ) reaches its reference value after



**Fig. 8.** Simulation result for half-bridge version of proposed converter. Horizontal axis is Time (s)

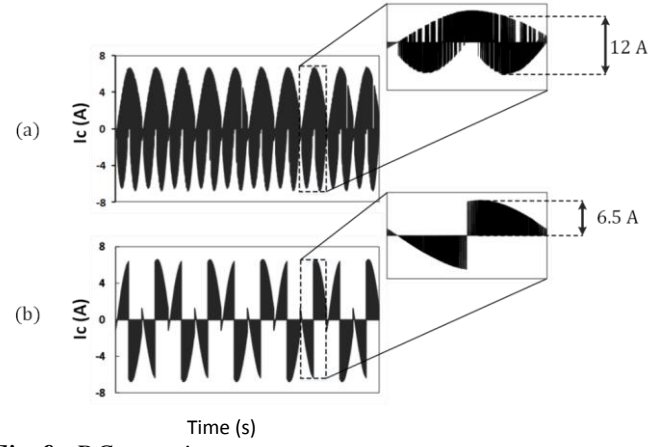
- a Output current,
- b Source current,
- c DC capacitor voltage,
- d Filtered voltage of shunt converter,
- e Filtered voltage of output converter,
- f Filtered output voltage

200 ms.

In order to show the performance of the converter in different conditions, simulation of the converter at two different output frequencies is carried out. As indicated in Figs. 5b and 5c, the converter supplies a load at frequencies of 25 and 400Hz which is prevalent in military and industrial applications. It can be verified that despite of inductive load, input unity power factor is achieved in all output frequencies.

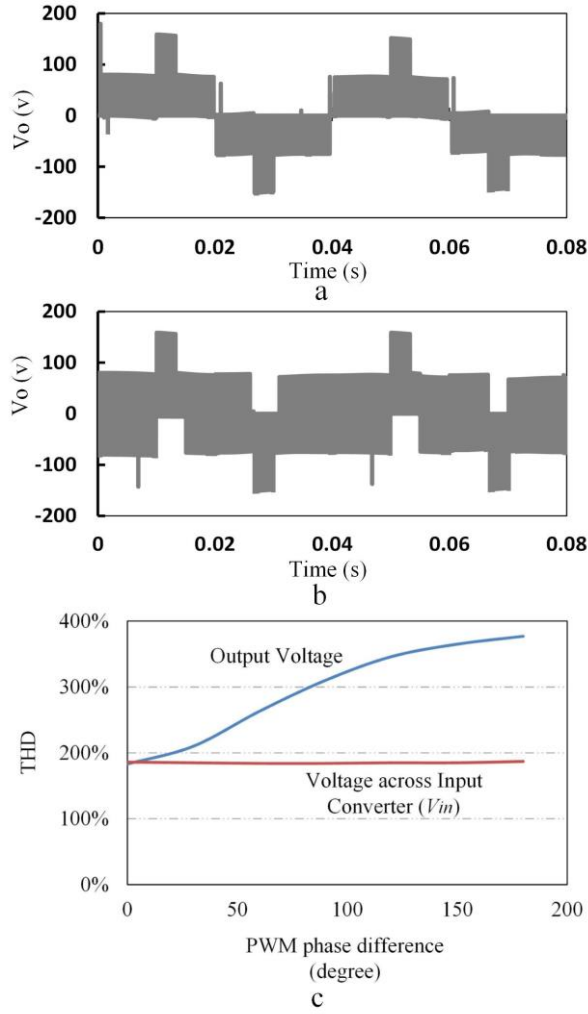
The value of each DC capacitor voltage is assigned in order to be capable to produce acquired ac voltage for each converter through (5). For instance, as long as Output Converter is considered, for producing an AC sine wave with amplitude of 40V across it, considering  $m_a=0.9$ , the value of DC capacitor,  $V_{dc}^{po}$ , is supposed to be greater than 44V, or  $40/m_a$ . similarly, as for Input Converter, although it is a current control converter, it needs to produce adequate AC voltage to manage its current. Owing to AC voltage across the Input Converter,  $v_o$ , which is considered to be 80Vp-p, the DC voltage of Input Converter,  $V_{dc}^{in}$ , is supposed to be greater than 40V. This rule is accurate for Shunt Converter: the AC voltage across this converter is  $v_s + v_o$  and the maximum of this term is about 60V (considering 40V amplitude for both  $v_s$  and  $v_o$ ) so the DC voltage of Shunt Converter,  $V_{dc}^{sh}$ , should be greater than 60V.

Fig. 6 shows the simulation which is carried out to demonstrate the effect of R-L and pure inductive load to the operation of the converter. As verified in simulation and proved previously in section 2, phase difference between voltage and current does not affect the operation of the converter. As the load becomes more inductive, the consumption active power reduced, so the amplitude of

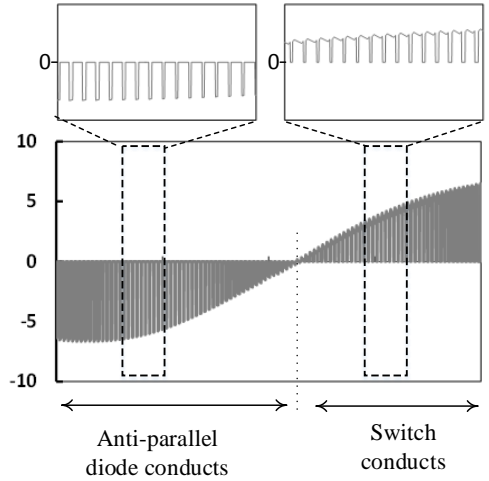


**Fig. 9.** DC capacitor currents,  
a Back-to-back,  
b Proposed T converter

input current,  $i_s$ , will be reduced. Fig. 6b shows pure inductive load so  $i_s$  gains small value.



**Fig. 10** Effect of PWM asynchronous  
a Output voltage when PWM modulators are synchronous  
b Output voltage when PWM modulators are not synchronous  
c The effect of PWM phase difference on output voltage THD



**Fig. 11** Current in Output Converter Switch

**Table 1** Prototype Ratings

Element	Rating
Supply Voltage	80Vp-p, 50Hz
Output Voltage	80Vp-p, 25Hz
Interface Reactor	4mH/10A RMS
Load	6Ω resistor in series with an 4mH Inductor
Switching Frequency	5KHz and 15KHz
Switching Elements	MOSFETs 20A/100V
DC Link Capacitors	4.7mF/100V
DC Voltages	
Input Converter	60 VDC
Output Converter	60 VDC
Shunt Converter	80 VDC

#### 4.2 Simulation results for Multi-level topology

In order to verify the multilevel type of the converter which can be used for high power application, a 5-level prototype of the proposed converter is simulated. Two series H-bridge blocks which make a 5-level converter, are used in each branches of T. Simulations are performed in steady state 25-Hz output frequency with an R-L load. For other output frequencies the results are similar



and are not repeated here. Fig. 7a shows the load voltage and current waveforms. Also Shunt Converter and Output Converter voltages are shown. Capacitor DC voltages of one of T branch converters are shown in Fig. 7b. It is shown that capacitor voltage balancing is done well. The number of cells is achieved through voltage restriction of each semiconductor switch. According to the overall DC voltage that is obtain by AC voltages and the semiconductor restrictions, the number of cells is specified.

#### 4.3 Simulation results for Half-Bridge type

As mention in previous sections, the proposed topology also is able to exploit half-bridge modules to reduce the number of switches. In this section, simulations confirm the accuracy of the operation of the topology of Fig. 3b. Like previous section, the results of Fig. 8 show the waveforms of the proposed converter including the source and load current and voltage, capacitor voltages, and the voltages of Shunt Converter and Output Converter. It is evident that voltage of branches are modulated switching voltages which consist of high frequency harmonics. To make these voltages clear to show, these voltages are passed through digital low pass filter and then placed in the paper.

As indicated in Fig. 8d and e, branch converters of T have DC component because it is not possible to reach negative values in half-bridge modules, but output voltage is a pure ac voltage. Inasmuch as DC components is omitted in loops of T. It is worth to mention that in order to reach pure AC in output terminals, all DC link voltages should be considered equal.

As for comparison to back-to-back converter, the proposed converter has a smaller capacitor current ripples at the same output power. Capacitor currents of both back-to-back and T-type converter are shown in Fig. 9. As shown in Fig. 9, the sudden change of capacitor current in T-type converter is half of the back-to-back one. This may increase the life time of capacitors. In fact, electrolytic capacitors have the least life time compared to other converter components. So by increasing the life time of capacitors, the reliability of the overall converter is increased.

All previous simulations is done while all PWM modulation signals are considered to be synchronous. In order to clarify the effect of asynchronous between PWM modulators, simulation of Fig. 10 is prepared. Since the operation of the proposed converter is independent of high frequency harmonics, the asynchronous signals do not affect the overall operation, but it affects the quality of output voltage: THD. As demonstrated in Fig. 10a, the output voltage, which is established when all PWM modulators are synchronous, has desired fundamental harmonics, 25Hz in this simulation, and the value of waveform THD is about 180%. In the other simulation, however, in which PWM modulator are not synchronous—90 degree phase between them in simulation of Fig. 10b—although

the output voltage waveform has desired fundamental frequency, the waveform quality has been deteriorated to higher THDs. As depicted in Fig. 10c, as the phase difference between sawtooth modulator signals increases, the THD of output voltage increases. In other words, although the synchronous of PWM signals is not mandatory for operation, but it should be considered to obtain the best performance.

It is obvious that the current of each loop also passes through Converters and hence through semiconductor switches as shown in Fig.11. This current should be considered to selection of suitable switches. As depicted in Fig. 11, free-wheeling diodes conduct in some time intervals especial when the converter supplies a R-L load. The more inductive load, the more time intervals that free-wheeling diodes conduct.

## 5. Experimental results

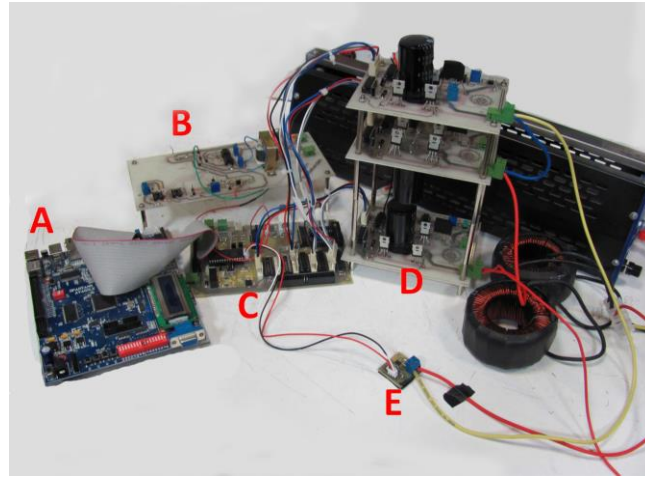
To verify the proposed topology and its control strategies, as shown in Fig. 12, a low power 3-level experimental prototype has been built. The converter supplies a load at constant amplitude and frequency i.e. as a power supply. The parameters and the rating of experimental prototype are same as in Table 1.

As shown in Fig. 12, the proposed converter is controlled through FPGA-Spartan6 from Xilinx controller board. The switching frequency of Output and Shunt Converter is 5-KHz and the switching frequency of Input Converter is 15-KHz. The hysteresis band current controller [38, 39] is also implemented on the FPGA controller board. An auxiliary board is used for synchronization and reference signal generation.

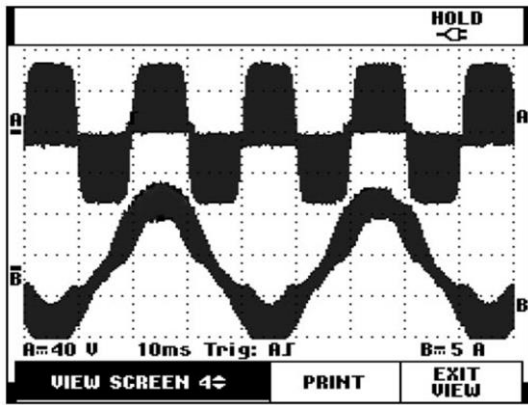
The results, as depicted in Fig. 13a-d, consist of output current at 25Hz, Output and Shunt Converter's voltage and current, and input source voltage and current. Fig. 13a shows the voltage and current of Output Converter which are obviously at different frequencies. Because the load and the Output Converter are in series, the output current also flows through the Output Converter, so, Fig. 13a also shows the output current in 25Hz. Fig. 13b shows the voltage and current of Shunt Converter which each of them has both 25-Hz and 50-Hz frequencies. As shown in Fig. 13c, the input voltage and current are in phase and at the same frequency so high power factor is achieved. Due to the inductance made from wiring of 50-Hz grid to the converter, the switching frequency is obvious in input voltage.

Finally In order to show the transient stability of the system, the start-up transient voltage of capacitors are shown in Fig. 13d which verify the stability performance of the converter during starting up of capacitor voltages. Digital voltage regulation controllers, implemented through FPGA

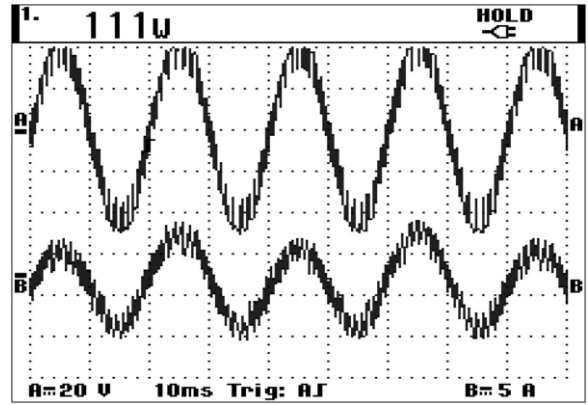
architecture, are designed slow because the effective selection of coefficient wasn't the aim of this paper. The results are captured through a Fluke digital scope which has two isolated input channel.



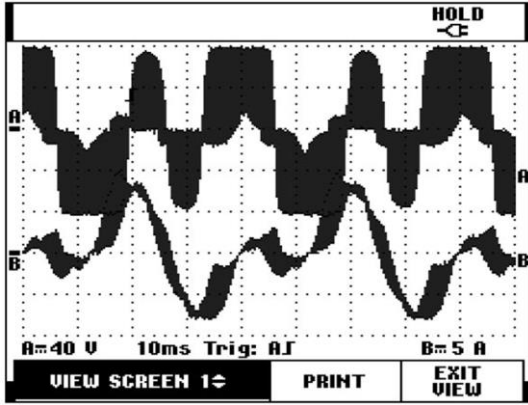
**Fig. 12.** Experimental Prototype, A: FPGA, B: Synchronizer and Ref. Gen. C: Interface Board, D: Power Converters, E: Current Sensor



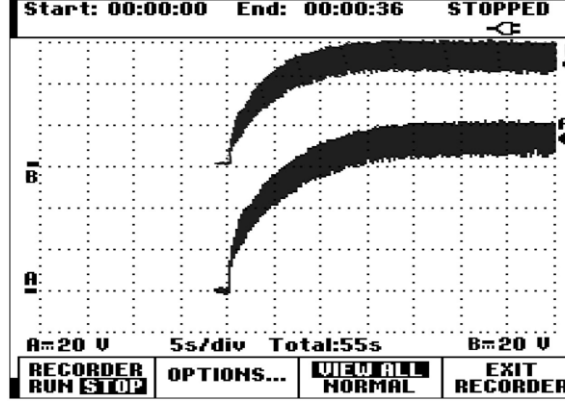
a



c



b



d

**Fig. 13** Waveforms of experimental results

- a Current and voltage of Output Converter:  $i_{po}$ ,  $v_{po}$ . Channel A: 40V/div, Channel B: 5A/div, Time: 10ms/div
- b Current and voltage of Shunt Converter:  $i_{sh}$ ,  $v_{sh}$ . Channel A: 40V/div, Channel B: 5A/div, Time: 10ms/div
- c Current and voltage at input terminal:  $i_s$ ,  $v_s$ . Channel A: 20V/div, Channel B: 5A/div, Time: 10ms/div
- d Start up capacitor voltages of A: Shunt Converter:  $V_{dc}^{sh}$ , B: Output Converter:  $V_{dc}^{po}$ . Channel A: 20V/div, Channel B: 20V/div, Time: 5s/div

## 6. Conclusion

In this paper a novel frequency changing converter with high input power factor and output voltage regulation has been proposed. The converter, in its basic form, consists of three H-bridges—namely Shunt Converter, Output Converter, and Input Converter—that are placed in branches of a T-type structure as its building blocks. Appropriate control scheme was carried out to handle the proposed converter as a power supply. This includes schemes that are suitable for: regulation of all capacitor voltages; tracking of the Input Converter current; and setting of the voltages of the Shunt Converter and Output Converter.

In comparison to conventional back-to-back frequency changing converters, the proposed T converter has lower sudden change in amplitude of DC-link capacitor current hence the life time of electrolytic capacitor has been improved.

Two other modified structures are driven using half-bridge and cascaded H-bridges as the building blocks in each branches of T. Using MMC in each branch results in a multilevel version of the converter which is suitable for high power applications. This enables a modular implementation approach in which voltage and power rating, can be expanded to higher values for high power applications. Using this structure, requirement for multi-winding low-frequency transformer, used in multilevel AC/AC systems, is eliminated, because there is no DC link short circuit intervals and isolation is not necessary, hence the weight and cost of the overall converter are reduced. By using half-bridge inverters in the branches of T, a unity power factor frequency changing converter is constructed with only six switching devices. Also by simulation, the correct operation of the multilevel version and the half-bridge version of the proposed topology, in steady state, has been shown.

Operation of proposed topology as a power supply with a specified output voltage and frequency was successfully carried out in simulation and experimental prototype. Experimental results also confirms the performance of the proposed T-type converter even under all non-idealities and its well performance through starting up and establishing capacitor voltages at desired values.

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